ABSTRACT

A memory cell array comprises a two dimensional array of memory cells fabricated on a semiconductor substrate. The memory cells are arranged in a plurality of rows and a plurality columns. Each column of memory cells comprising a plurality of alternating channel regions and source/drain regions. A conductive interconnect is positioned above each source/drain region and coupled to only one other source/drain region. The one other source/drain region is in a second column that is adjacent to the column. The conductive interconnects are positioned such that every other conductive interconnect connects to the adjacent column to a right side of the column and every other conductive interconnect connects to adjacent column to the left side of the column. A plurality of source/drain control lines extends between adjacent columns of memory cells and electrically couples to each conductive interconnect that couples between the adjacent columns.